IN THE SPECIFICATION:

Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date) please replace paragraph numbers **[0003], [0005], [0008], [0009], [0010], [0011], [0014], [0018], [0019], [0020], [0021], [0025], [0026], [0027], [0030], [0031], [0032], [0033], and [0034].** A marked-up version to clearly identify amendments to the specification as required by 37 C.F.R. § 1.121(b)(3)(iii) is attached.

[0003] Consumers want their portable devices to perform the same functions as their desktop computers, therefore requiring large amounts of memory in a much smaller electronic device. One way of accomplishing this is to increase the density of a semiconductor die package by using the package's real estate more efficiently. One advantage of high density packaging is that it decreases the length of the connections between the semiconductor die and the package, allowing the semiconductor die to respond faster. Also, reducing the length of the connections reduces the signal propagation time and makes the signal paths less vulnerable to the affects of noise.

[0005] A multichip module comprised of stacked semiconductor dice is disclosed in United States Patent 5,323,060, issued to Fogal et al. The semiconductor dice are electrically connected to a substrate by extending long bond wires from bond pads on each semiconductor die to the substrate. In order to accommodate the loop height of the bond wires, a thick adhesive layer is applied between the semiconductor dice. The adhesive layer must be thick enough that the bond wires of the lower semiconductor die do not contact the upper semiconductor die. This multichip module is not suited for small electronic devices because the adhesive layer between the dice increases the overall thickness of the semiconductor package.

[0008] In United States Patent 5,994,166 issued to Akram et al. a dense semiconductor package comprising multiple substrates with attached flip-chips is disclosed. The substrates are stacked on top of one another. Column-like connections positioned between the stacked substrates provide electrical communication. The electrical connections must be of sufficient

height to provide enough clearance between substrates to mount components and also must be of sufficient strength to provide support between the substrates. Since the column-like connections cause unused space between the substrates, this semiconductor package is incompatible with electronic devices that require small semiconductor packages.

[0009] While numerous high density semiconductor packages exist, they share a common disadvantage in that they inefficiently use the space of the semiconductor package. The unused or wasted space may be the result of thick adhesive layers between semiconductor dice or may be caused by rigid interposers or other spacers. Small electronic devices, such as cell phones and PDAs, have very limited space and cannot afford to waste any of this space. Reducing the wasted or unused space in a semiconductor die package is essential because large packages occupy too much of this limited space. It would be preferable to reduce the unused or wasted space in a stack of semiconductor dice by more closely spacing the semiconductor dice. It would be more preferable for the semiconductor dice to be spaced substantially one on top of another. It would be most preferable for the overall size of a high density semiconductor package to be caused only by the thickness of the semiconductor die and a substrate, without substantial thickness coming from additional packaging or unused space.

[0010] Methods for connecting dice to a substrate are well known in the art. For example, wire bonding, tape automated bonding ("TAB"), and controlled collapse chip connection ("C4") are commonly used to physically and electrically connect semiconductor dice to a substrate. Wire bonding utilizes fine wire conductors bonded on one end to the substrate and on the other end to electrical contacts on the semiconductor die. Because wire bonding requires wires to be welded to the die, there must be adequate space to accommodate the wires. TAB utilizes patterned metal on a polymeric tape to join dice together. The joined semiconductor dice are attached to a substrate by outer lead bonding. C4, or flip-chip, bonding uses solder balls on the surface of a semiconductor die to bond the semiconductor die to a substrate.

[0011] In addition to the above-mentioned methods, the prior art also discloses using vias to attach a semiconductor die to a substrate and to provide electrical communication

between the semiconductor die and substrate. The vias may be filled with conductive metal or flexible leads may be run through the vias to provide electrical communication. As mentioned above, United States Patent 5,128,831 issued to Fox, III et al. teaches a high density package composed of multiple submodules, each of which contain a chip bonded to a substrate. Each substrate has a metallization pattern, which comprises multiple conductive traces. A spacer is adhesively bonded to the peripheral upper surface of each submodule before the submodules are stacked. Both the substrate and spacer contain vias that are coincident and substantially coaxial to each other when the package is assembled. The vias are filled with solder to electrically connect the traces of all the submodules. Similarly, United States Patent 5,148,266 issued to Kane et al., mentioned in more detail below, uses solid vias to electrically interconnect two chips on opposite sides of a flexible carrier.

[0014] In United States Patents 5,148,266 and 5,682,061 issued to Khandros et al., a semiconductor chip assembly containing an interposer and flexible leads is disclosed. The interposer separates a semiconductor chip and a substrate. The chip and substrate electrically communicate through flexible leads that run through apertures in the interposer. The leads connect the chip to terminals on the interposer, which are then connected to contact pads on the substrate. The flexible leads allow for movement of the contacts on the chip and, therefore, reduce the stresses caused by thermal cycling.

[0018] While the above-mentioned inventions disclose flexible components in semiconductor die packages, they only disclose attaching one semiconductor die to a substrate. Since high density semiconductor packages are necessary for new generations of electronic devices, it would be preferable to combine flexible components with semiconductor die packages that can accommodate multiple semiconductor dice.

[0019] United States Patent 5,252,857 issued to Kane et al., discloses both of these features. A dense memory package is disclosed where two memory chips are mounted face-to-face on opposite sides of a flexible carrier or interposer. The two chips contain solder bumps that align when the chips are placed face to face. In addition, the interposer contains pads that are

coated with low melting point solder. The bumps on the chips contact the pads on the interposer and are soldered together. Kane also discloses a plurality of pairs of chips mounted on opposite sides of a flexible carrier. The flexible carrier with the attached chips can be folded to connect with substrates, such as printed circuit boards. While Kane discloses a flexible carrier that can be used to connect multiple die to a printed circuit board or backplane, Kane discloses that the pairs of dice are mounted face-to-face on opposite sides of the flexible carrier.

[0020] The present invention solves the above-mentioned problems. The present invention discloses a high density semiconductor package that has reduced or eliminated the unused space between stacked semiconductor die. The resulting high density semiconductor package of the present invention is small, and is, therefore, useful in portable electronic devices such as cell phones and PDAs.

[0021] The present invention relates to a folded interposer and a high density semiconductor package that utilizes the folded interposer. The folded interposer is comprised of a thin, flexible material that can be folded around one or multiple semiconductor dice. The folded interposer allows multiple semiconductor dice to be efficiently stacked in a high density semiconductor package by reducing the unused or wasted space between stacked semiconductor dice. The present invention also relates to a method of packaging semiconductor dice in a high density arrangement and a method of forming the high density semiconductor die package. Finally, the present invention relates to a computer system that incorporates the folded interposer in a high density semiconductor die package.

[0025] FIG. 3 is a side view of an interposer of the present invention folded around two semiconductor dice;

[0026] FIG. 4 is a side view of an interposer of the present invention folded around two semiconductor dice and attached to a substrate;

[0027] FIG. 5 is a side view of an interposer of the present invention folded in a serpentine fashion around more than two semiconductor dice; and

[0030] As illustrated in drawing FIGS. 2 and 3 the interposer **10** is flexible enough to fold around one or multiple semiconductor dice **12**. Preferably, the semiconductor dice **12** are bare, unpackaged die. As is illustrated in drawing FIG. 2 (vias not shown), the interposer **10** surrounds at least three sides of one semiconductor die **12**, to form an intermediate packaging structure **28**. Illustrated in drawing FIG. 3 (vias not shown) is an intermediate packaging structure **28** containing multiple semiconductor dice **12**, wherein the interposer **10** surrounds at least two sides of each semiconductor die.

[0031] Methods of attaching a semiconductor die to a substrate are well known in the art. Any means known in the art for attaching the semiconductor die to the interposer may be used in the present invention. Intermediate packaging structure **28**, which includes the interposer **10** and attached semiconductor die **12**, is attached to a substrate to form a high density semiconductor package **14** (see FIG. 4).

[0032] The present invention also relates to a high density semiconductor die package **14** utilizing the folded interposer **10**. As is best illustrated in drawing FIGS. 4 through 6, the folded interposer **10** is used to attach one or multiple semiconductor dice **12** to a substrate **22**, thus forming the high density semiconductor package **14**. The interposer **10**, which has two surfaces, is folded around the semiconductor die **12** to form intermediate packaging structure **28**. As is best illustrated in drawing FIG. 2 (vias not shown), the interposer **10** surrounds at least three sides of one semiconductor die **12** in intermediate packaging structure **28**. Illustrated in drawing FIG. 3 (vias not shown) is an intermediate packaging structure **28** containing two semiconductor dice **12**, wherein the interposer **10** surrounds at least two sides of each semiconductor die. Since the bond pads **26** of each semiconductor die must be in contact with vias **24**, multiple semiconductor die **12** must be positioned in groups of two in a back-to-back configuration so that all semiconductor die **12** are in electrical communication with substrate **22**.

Intermediate packaging structure **28** is then attached to the substrate **22** through the electrical contacts **20** on the first surface **16** of the interposer. The substrate **22** may be any type of semiconductor substrate known in the art, such as a printed circuit board. The semiconductor die **12** and substrate **22** are in electrical communication through the bond pads **26** and the electrical contacts **20**, which are in contact with the vias **24**. The vias **24** may be filled with a conductive material to provide electrical communication between the semiconductor die **12** and substrate **22**.

[0033] The high density semiconductor die package **14** accommodates more than two semiconductor die by weaving the flexible interposer **10** around groups of two semiconductor dice. Since the bond pads **26** of each die must be in contact with vias **24**, the two semiconductor dice **12** must be positioned in a back-to-back configuration so that all semiconductor dice **12** are in electrical communication with substrate **22**. As is illustrated in drawing FIG. 5 (bond pads and vias not shown), the interposer weaves in a serpentine fashion between groups of two semiconductor dice.

[0034] As is illustrated in drawing FIG. 5 (bond pads, vias, and substrate not shown), the present invention also relates to a method of packaging semiconductor dice in a high density arrangement. The semiconductor dice are packaged by providing at least one semiconductor die **12**, a flexible interposer **10**, and a substrate **22**. The interposer **10** is folded around and attached to the semiconductor dice **12**. The interposer **10** has a first surface **16**, a second surface **18**, and vias **24** that extend through the interposer **10** from the first surface **16** to the second surface **18**. The first surface **16** includes electrical contacts **20**. The semiconductor dice **12** are attached to the interposer **10** through bond pads **26** on the active surface of the semiconductor die **12** to form intermediate packaging structure **28**. Intermediate packaging structure **28** is then attached to substrate **22** through the electrical contacts **20** to form a high density semiconductor package **14**. This attachment also results in electrical communication between the semiconductor die **12** and the substrate **22**. In a high density semiconductor package **14** containing one semiconductor die **12**, the interposer **10** is folded around the

semiconductor die **12** so that at least three sides of the semiconductor die are surrounded, as is illustrated in drawing FIG. 2 (vias and substrate not shown). In a high density semiconductor package **14** containing two semiconductor dice **12**, the interposer **10** surrounds at least two sides of each semiconductor die **12**, as is illustrated in drawing FIG. 3 (vias and substrate not shown). Illustrated in drawing FIG. 5 (bond pads, vias, and substrate not shown) is that the interposer **10** weaves in a serpentine fashion between semiconductor die **12** stacked in groups of two when a high density semiconductor package **14** containing more than two semiconductor dice **12** is desired. Additionally, electrical contacts **20** may be applied to a top surface **30** of the package **14**, as is shown in drawing FIG. 6 (bond pads, vias, and substrate not shown), so that the package **14** can be attached to other semiconductor devices, depending on the desired application.